IN THE CLAIMS

1-14 (Cancelled)

15. (Previously Presented) The process of claim 16, comprising forming an oxide over said bitlines.

16. (Currently Amended) A process of fabricating a memory cell comprising a substrate that comprises a first region and a second region with a channel therebetween, the method comprising:

forming a gate above said channel of said substrate, wherein said gate comprises a single polysilicon layer;

forming bitlines on both sides of said gate subsequent to said forming said gate comprising said single polysilicon layer; and

siliciding said bitlines.

17. (Currently Amended) The process of claim 16, comprising siliciding said single polysilicon layer.

18. (Currently Amended) The process of claim 16, wherein said siliciding of said bitlines and said single polysilicon layer occur simultaneously.

19. (Previously Presented) The process of claim 16, comprising:

forming a charge trapping region that contains a first amount of charge; and

forming a layer between said channel and said charge trapping region, wherein said layer has a thickness such that said first amount of charge is prevented from directly tunneling into said layer.

20. (Original) The process of claim 19, wherein said charge trapping region comprises silicon nitride.

21. (Previously Presented) The process of claim 16, wherein said gate comprises an N-type material.

22. (Original) The process of claim 21, wherein said gate comprises a polycrystalline silicon.

23. (Original) The process of claim 19, further comprising forming an insulating layer on said charge trapping region.

24. (Original) The process of claim 23, wherein said insulating layer comprises silicon dioxide.

25. (Original) The process of claim 24, wherein said charge trapping region comprises silicon dioxide.

26. (Previously Presented) The process of claim 16, wherein said memory cell comprises an EEPROM memory cell.

27. (Previously Presented) The process of claim 16, wherein said memory cell comprises a two-bit memory cell.

28. (Previously Presented) The process of claim 16, wherein said substrate comprises a P-type substrate.

29. (Previously Presented) The process of claim 16, further comprising scaling the length of said bitlines.

30. (Previously Presented) The process of claim 29, wherein said scaling comprises reducing the thermal cycle of said bitlines.